

In the Claims:

Please make the following revisions to the claims:

1. (Original) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising the steps of:
providing a substrate having a gate structure formed thereon;
forming a dielectric spacer layer over the semiconductor substrate; and
etching said dielectric spacer layer, prior to forming a layer subsequent to the dielectric layer, to form L-shaped spacers.
2. (Amended) The method of ~~Item~~Claim 1, further including the step of forming a liner oxide layer over said gate structure prior to the step of forming the dielectric spacer layer.
3. (Amended) The method of ~~Item~~Claim 2 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.
4. (Amended) The method of ~~Item~~Claim 1 wherein said dielectric spacer layer comprises a nitride layer.
5. (Amended) The method of ~~Item~~Claim 3, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.
6. (Amended) The method of ~~Item~~Claim 1 wherein said dielectric spacer layer comprises a silicon oxynitride layer.
7. (Amended) The method of ~~Item~~Claim 1 wherein the step of etching said dielectric layer includes anisotropically etching said dielectric layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

8. (Amended) The method of ~~Item~~Claim 7, wherein said and horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.
9. (Amended) The method of ~~Item~~Claim 7 wherein said dielectric layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH₃F and O₂ in combination with an inert gas to form said L-shaped spacers.
10. (Amended) The method of ~~Item~~Claim 7, wherein said dielectric layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH₃F and O₂ in combination with an inert gas.
11. (Amended) The method of ~~Item~~Claim 1, wherein the step of etching said dielectric layer to form said L-shaped spacers includes using CH₃F and O₂ chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH₃F to O₂.
12. (Amended) The method of ~~Item~~Claim 11, wherein the step of etching said dielectric layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.
13. (Amended) The method of ~~Item~~Claim 11, wherein the step of etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.
-
14. (Withdrawn) An apparatus comprising a first transistor structure including an L-shaped spacer having a vertical portion varying substantially in thickness over a majority of its length and a horizontal portion varying substantially in thickness over a majority of its length.

15. (Withdrawn) The apparatus of Item 14, wherein said vertical and horizontal portions of L-shaped spacers have a bulging profile which varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.
16. (Withdrawn) The apparatus of Item 14, wherein the length of the horizontal portion of the L-shaped spacer ranges from approximately 80 percent of the deposition thickness to 150 percent of the deposition thickness.
17. (Withdrawn) The apparatus of Item 14 further comprising:
a second transistor immediately adjacent to the first transistor, where in a distance between a sidewall portion of a gate of the first transistor and a sidewall portion of a gate of the second transistor less than 120 nanometers.
18. (Original) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising the steps of:
providing a substrate having a gate structure formed thereon;
forming a liner oxide layer on said gate structure;
forming a dielectric spacer layer over said liner oxide layer; and
anisotropically etching said dielectric layer, prior to forming a layer subsequent to the dielectric layer, to form L-shaped spacers, said L-shaped spacers having vertical portions and a horizontal portion, wherein the horizontal portion varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.